UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,406	10/29/2003	Russell W. Guenthner	52003218	7204

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EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
06/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/697,406	GUENTHNER ET AL.
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2007*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All b)☐ Some * c)☐ None of:

　　1.☐ Certified copies of the priority documents have been received.

　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to application 10/697,406 and response filed on

4/3/2007. Claims 1-6 remain pending in the application.

Response to Amendment

1.   The affidavit filed on 10/2/2006 under 37 CFR 1.131 has been received on 4/3/07

and is sufficient to overcome the Beraudo et al. reference dated June 2003.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Togawa

et al., "A Performance-Oriented Circuit Partitioning Algorithm with Logic-Block

Replication for Multi-FPGA Systems," IEEE, Nov. 1996, pages 294-297.

4.   As to claim 1, Togawa et al. teach substantially the same claimed invention of a

method for optimizing timing performance of an overall logic circuit implemented in a

Field Programmable Gate Array (FPGA) with at least one programmable interconnect

routed from a source to a specific load affected negligibly by fanout to other loads

connected to the same source (pages 294-297) comprising the steps of a) synthesizing

the overall logic for a first implementation in the FPGA, the synthesis including `·

construction and a first placement of one or more logic functions on the FPGA (at least

see Fig. 2a; b) analyzing the timing paths of the first implementation with the first

placement (at least see Fig. 2a); c) determining one or more critical timing paths from

analysis of the first implementation (at least see Fig. 2a); d) selecting as an object for

improvement a specific critical timing path from the critical timing paths (object b); e)

implementing in a new way the critical logic in the selected specific critical timing path

with the implementation of the critical logic performed with relative disregard as the

fanout of signals to other loads in the overall logic circuit and with the placement of logic

functions in the selected specific critical path designed primarily to minimize the

interconnected routing distance of the signals contributing to that selected specific

critical path, such implementation being operatively substituted for the first placement

and being a selection of new logic elements to implement the selected specific critical

path, with said selection of new logic elements being a duplication (replication) of logic

elements utilizing in the first placement but forming a second placement of the logic

functions on the FPGA, those new logic elements of the second placement placed in a

more optimal placement than the first placement for minimizing the interconnected

routing distance of the selected specific critical path (at least see Fig. 2b) (see detailed

pages 294-297). Fig. 2a-b show the claim invention, where i3 is a common input source

to different output loads. Critical path delays are detected. Fig. 2b shows the result,

where a circuit element b is selected for duplication in order to minimize critical path

delay to meet delay constraint. The process is repeated for all critical path delays within

the IC design. Therefore, the claimed limitations are anticipated by the article to

Togawa et al..

5.   As to claim 2, Togawa et al. teach the implementation of the critical logic in said

new way in step e) is limited only to changes in the placement of the logic elements in

the selected specific critical path (at least see Fig. 2a-b, pages 294-297)).

6.   As to claim 3, Togawa et al. teach f) modifying the second placement of logic

functions in the overall logic circuit to accommodate the changes in placement of the

selected specific critical path while maintaining approximately the new placement of the

critical logic; g) repeating steps b) through e) of claim 1,where the last implementation

and placement of the overall logic circuit from step e) becomes the basis for starting

again with the last implementation becoming the basis implementation (at least see Fig.

2a-b, pages 294-297). Note that in order to achieve an optimized overall timing

performance of a logic circuit, repeating process must be done for all critical paths in the

logic circuit.

7.   As to claim 4, Togawa et al. teach the implementation of the critical logic in said

new way in step e) is limited only to changes in the placement of the logic elements in

the selected specific critical path (Fig. 2a-b; pages 294-297).

8.   As to claim 5, remarks set forth in rejection of claim 1 equally applied because of

substantially same claimed limitations.

9.   As to claim 6, Togawa et al. teach repeating steps c) through f) where the

placement resultant from step f) becomes the timing path used in step c). Note that in

order to achieve an optimized overall timing performance of a logic circuit, repeating

process must be done for all critical paths in the logic circuit.

Remarks

10.   Applicants' arguments have been considered, but they are not persuasive.

Mainly, applicants argued that Togawa described a multi FPGA chips and not work on a

single FPGA. Examiner disagrees. Togawa teaches an algorithm that resolves all path

delay constraints by means of effective logic-block replication in the detected

constrained paths (see page 279; Fig. 2). Although, Togawa described that the

algorithm applied on a multiple FPGA chips, it would also apply on a single FPGA chip.

The replication of logic blocks on the detected delay constraints, where the detected

delay constraints can be on the same chip or on a multiple chips. In addition, the

partitioned logic blocks can be on the same chip or on a multiple chips. Resolving all

delay paths violated delay constraints can be applied on a single FPGA chip or on a

multiple FPGA chips by means of replication of logic blocks on the detected delay path

constraints. This can be shown clearly in Fig. 2. The replication of logic blocks resolved

all delay paths violated delay constraints whether on a single FPGA or on a multiple

FPGA chips because the replication of logic blocks would minimized interconnections

as shown in Fig. 2. Therefore, the claimed invention is anticipated by the teachings of

Togawa.

11.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, AU: 2825